| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 3690 | (fabricat$6 or making or make$3 or forming) adj6 ((image$3 or imaging) adj3 (sensor$2 or sensing)) | USPAT; EPO; JPO; DERWENT | OR | ON | 2005/06/09 14:40 |
| L2 | 49 | ((fabricat$6 or making or make$3 or forming) adj6 ((image$3 or imaging) adj3 (sensor$2 or sensing))) near25 (isolat$6 or trench$6 or groove$3) | USPAT; EPO; JPO; DERWENT | OR | ON | 2005/06/09 14:42 |
| L3 | 437 | (image or imaging) and (depletion) and (buffer$6) and (transistor$2) and (etch$6) and (region$2) | USPAT; EPO; JPO; DERWENT | OR | ON | 2005/06/09 15:26 |
| L4 | 270 | ((nitrid$3) near4 (layer$2 or pad$2)) and ((deplet$6 adj3 mode) near3 (transistor$2)) | USPAT; EPO; JPO; DERWENT | OR | ON | 2005/06/09 14:47 |
| L5 | 11 | 3 and 4 | USPAT; EPO; JPO; DERWENT | OR | ON | 2005/06/09 14:52 |
| L6 | 1 | 2 and 5 | USPAT; EPO; JPO; DERWENT | OR | ON | 2005/06/09 14:48 |
| L7 | 1 | 2 and 3 | USPAT; EPO; JPO; DERWENT | OR | ON | 2005/06/09 14:55 |
| L8 | 1533 | ((isolat$6) near3 (layer$2 or substrat$3)) near6 (trench46 or groove$2) | USPAT; EPO; JPO; DERWENT | OR | ON | 2005/06/09 14:56 |
| L9 | 0 | 2 and 8 | USPAT; EPO; JPO; DERWENT | OR | ON | 2005/06/09 14:56 |
| L10 | 3 | 4 and 8 | USPAT; EPO; JPO; DERWENT | OR | ON | 2005/06/09 15:01 |
| L11 | 1 | "4101788".PN. | USPAT; USOCR | OR | ON | 2005/06/09 14:59 |
| L12 | 1 | "4028556".PN. | USPAT; USOCR | OR | ON | 2005/06/09 15:00 |
| L13 | 342 | (method$3) adj4 ((making or fabricat$6) near4 ((image$3 or imaging) adj3 (sensor or sensing))) | USPAT; EPO; JPO; DERWENT | OR | ON | 2005/06/09 15:04 |
| L14 | 2 | 4 and 13 | USPAT; EPO; JPO; DERWENT | OR | ON | 2005/06/09 15:05 |

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L2: (49) ((fabricat$6 or making or make$3 or forming) a...
L3: (437) (image or imaging) and (depletion) and (buffer...
L4: (270) ((nitrid$3) near4 (layer$2 or pad$2)) and ((dep...
L6: (1) 2 and 5
L5: (11) 3 and 4
L7: (1) 2 and 3
L8: (1533) ((isolat$6) near3 (layer$2 or substrat$3)) nea...
L9: (0) 2 and 8
L10: (3) 4 and 8
L11: (1) "4101783".PN.
L12: (1) "4028556".PN.
L13: (342) (method$3) adj4 ((making or fabricat$6) near...
L15: (0) 8 and 13
L14: (2) 4 and 13
L16: (1) "4484210".PN.
L17: (1) "4527182".PN.
L18: (1) "4984047" PN
L19: (1) "5051797".PN.

Default Operator: OR

3 and 4

| | U | 1 | Document ID | Issue Date | Pages | Title | Current OR | Current XRef | Retrieval Class | Inventor |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | ☐ | ☐ | US 6222210 B1 | 20010424 | 52 | Complementary heterostructure integrated single metal transistor | 257/194 | 257/E21.697; 257/E27.012; | | Cerny; Charles L. A. |
| 2 | ☐ | ☐ | US 6198118 B1 | 20010306 | 53 | Complementary heterostructure integrated single metal transistor | 257/194 | 257/192; 257/195; | | Cerny; Charles L. A. |
| 3 | ☐ | ☐ | US 6184055 B1 | 20010206 | 18 | CMOS image sensor with equivalent potential diode and method for | 438/57 | 257/233; 257/292; | | Yang; Woodward et |
| 4 | ☐ | ☐ | US 6180969 B1 | 20010130 | 17 | CMOS image sensor with equivalent potential diode | 257/291 | 257/292; 257/E27.128; | | Yang; Woodward el |
| 5 | ☐ | ☐ | US 5686857 A | 19971111 | 8 | Zero-crossing triac and method | 327/451 | 327/452; 327/465 | | Heminger; David M. |
| 6 | ☐ | ☐ | US 5015594 A | 19910514 | 15 | Process of making BiCMOS devices having closely spaced device regions | 438/207 | 148/DIG.9; 257/370; | | Chu; Shao-Fu S. et a |
| 7 | ☐ | ☐ | US 4806983 A | 19890228 | 23 | Flat-panel display and a process for its manufacture | 345/90 | 345/212; 349/149; | | Benjamin; John D. el |
| 8 | ☐ | ☐ | US 4527257 A | 19850702 | 13 | Common memory gate non-volatile transistor memory | 365/184 | 257/324; 257/E29.309; | | Cricchi; James R. |
| 9 | ☐ | ☐ | US 4472791 A | 19840918 | 30 | CMOS Unipolar nonvolatile memory cell | 365/181 | 365/182; 365/184 | | Haken; Roger A |
| 10 | ☐ | ☐ | US 4182023 A | 19800108 | 15 | Process for minimum overlap silicon gate devices | 438/301 | 148/DIG.131; 148/DIG.143; | | Cohen; Jerome et al |
| 11 | ☐ | ☐ | US 4149904 A | 19790417 | 12 | Method for forming ion-implanted self-aligned gate structure by controlled | 438/301 | 148/DIG.143; 148/DIG.53; | | Jones; Robert K. |

Ready                                                                                    RUN